ABSTRACT

A structure and apparatus is provided for an electrostatic discharge power clamp , for use with high voltage power supplies. The power clamp includes a network of transistor devices, for example, nFETs arranged in series between a power rail and a ground rail. The first transistor device is biased into a partially on-state, and thus, neither device sees the full voltage potential between the power rail and the ground rail. Accordingly, the power clamp can function in voltage environments higher than the native voltage of the transistor devices. Additionally, the second transistor device is controlled by an RC network functioning as a trigger which allows the second transistor device to turn on during a voltage spike such as occurs during an ESD event. The capacitor of the RC network may be small thereby requiring small real estate on the integrated circuit. The clamp may have fast turn-on times as well as conducting current for long periods of time after turning on.